

Programme's After Market Services

NHD-4 Series Transceivers

Chapter 5

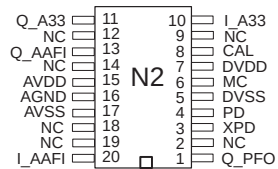
Schematics/Layouts & Pinouts

CONTENTS

	Page No
Pinouts	
BASEBAND FILTER	
IF + FM DETECTOR	5-3
2 x SYNTH	5-3
CDAGCR	5-4
MCU	5-5
MCU memory Flash EEPROM, SRAM	5-6
DSP memory	5-7
PSL + N500	6-7
CDAGCT4	5-8
CDCONT5	5-9
CDRFI	5-10
CDSB 4.5	5-11
AUDIO CODEC	5-13
DSP	5-14
Schematics / Layouts (GR1_17a)	
Figure 1. NHD-4 Block Diagram	5-15
Figure 2. Power Supply	5-16
Figure 3. MCU	5-17
Figure 4. DSP	5-18
Figure 5. CDMA Asic	5-19
Figure 6. CDRFI	5-20
Figure 7. Audio	5-21
Figure 8. I/O	5-22
Figure 9. MCU Memory	5-23
Figure 10. DSP Memory	5-24
Figure 11. RX	5-25
Figure 12. TX	5-26
Figure 13. Synth	5-27
Figure 14. RF Block	5-28
Figure 15. RFSW	5-29
Figure 16. Control	5-30
Figure 17. Component Layout –Top	5-31
Figure 18. Component Layout – Bottom	5-32
Figure 19. Component Values – Top	5-33
Figure 20. Component Values – Bottom	5-34

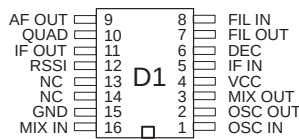
BASEBAND FILTER (N2) IF + FM DETECTOR (D1)

BASEBAND FILTER N2



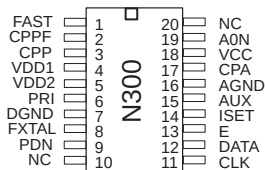
- | | |
|--------------------------------|---|
| 1 Capacitor Input (I-channel) | 11 Capacitor Input (Q-channel) |
| 2 RXI Output (I-channel) | 12 No Connection (Grounded) |
| 3 RX_FIL_CAL CALibration start | 13 Input (Q-channel) |
| 4 Digital VDD | 14 No Connection (Grounded) |
| 5 9.8304 MHz Master Clock | 15 Analog VDD |
| 6 Digital VSS | 16 Analog signal GrouND for external stablation |
| 7 Connected to Ground | 17 Analog VSS |
| 8 Power Down, Active low | 18 No Connection (Grounded) |
| 9 No Connection (Grounded) | 19 No Connection (Grounded) |
| 10 RXQ Output (Q-channel) | 20 Input (I-channel) |

IF AMP+FM DETECTOR D1

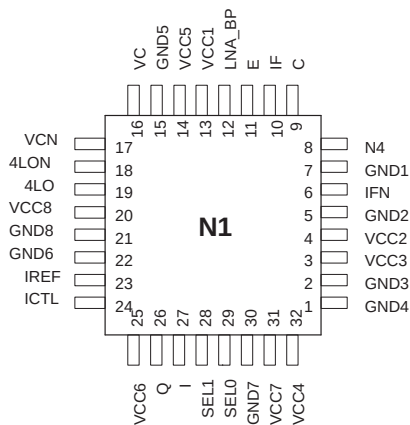


- | | |
|---------------------------|---|
| 1 Local oscillator input | 9 Demodulate signal output |
| 2 Local oscillator output | 10 Phase shift signal input of FM demodulator |
| 3 Mix output | 11 Output terminal of IF AMP |
| 4 Power supply | 12 Output is DC vs Signal level (RSSI) |
| 5 2nd IF input | 13 No Connection |
| 6 Decoupling for bias | 14 No Connection |
| 7 INVERTER AMP output | 15 GND |
| 8 INVERTER AMP input | 16 1st IF signal input |

2 x SYNTH (N300)



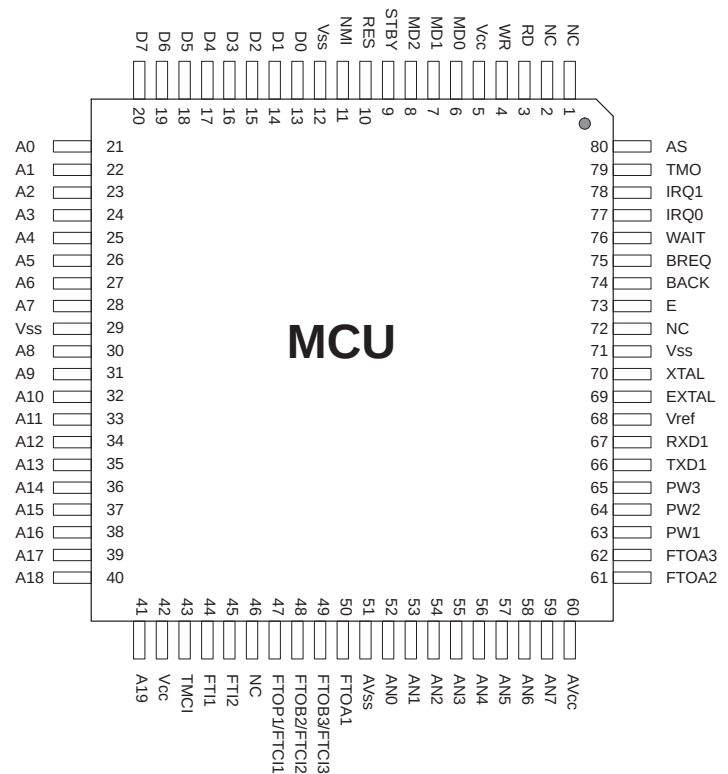
- | |
|--|
| 1 Control input to speed-up main synth |
| 2 Principal synth speed-up charge-pump output |
| 3 Principal synth normal charge-pump output |
| 4 Digital power supply 1 |
| 5 Digital power supply 2 |
| 6 1 GHz principal synth RF divider input |
| 7 Digital ground |
| 8 Common reference freq input from chrystal ascillator |
| 9 Principal synth power-on input |
| 10 No Connection |
| 11 Serial clock input |
| 12 Serial data input |
| 13 RX_LE Programming bus enable input (active LOW) |
| 14 Regulator pin to set the charge-pump currents |
| 15 Auxiliary synth frequency input |
| 16 Analog ground |
| 17 180MHz Auxiliary synth charge-pump output |
| 18 Supply for charge-pump and DAC circuits |
| 19 Auxiliary synth power-on input |
| 20 No Connection |

CDAGCR (N1)

- | | |
|---|---|
| 1 GROUND (Return for CCGA stage 3) | 51 Bypass for CCGA's control line |
| 2 GROUND (Return for CCGA stage 2) | 52 180° Clock Input |
| 3 DC power for CCGA stage 2 | 53 0° Clock Input |
| 4 DC power for CCGA stage 1 | 54 DC power for LO circuitry |
| 5 GROUND (Return for CCGA stage 1) | 55 GROUND (Return for LO circuitry) |
| 6 180° IF Input | 56 GROUND (Return for DeMod circuitry) |
| 7 GROUND (Return for LNA) | 57 Input control current reference |
| 8 Emitters of QC's | 58 Input control current |
| 9 Collector's of Q1 | 59 DC Power for DeMod circuitry |
| 10 Sets bias current for the internal LNA (short=6.2mA) | 60 Baseband 90° output |
| 11 Emitters of Q1 (Internal LNA) | 61 Baseband 0° output |
| 12 Bypass for LNA's bias line | 62 Set high for -14 dB change in total gain |
| 13 DC power for LNA | 63 Set high for -7 dB change in total gain |
| 14 DC power for gain control | 64 GROUND (Return for Outputs Buffers) |
| 15 GROUND (Return for Gain control) | 65 DC power for Output Buffers |
| 16 Bypass for CCGA's control line | 66 DC power for CCGA stage 3 |

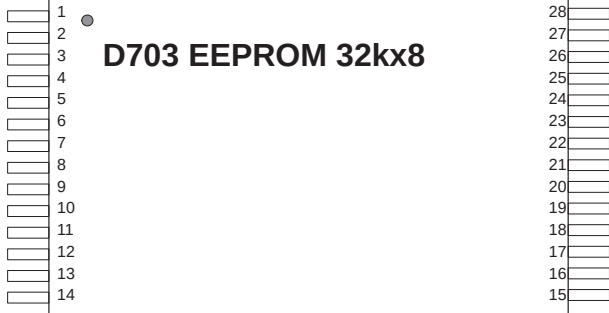
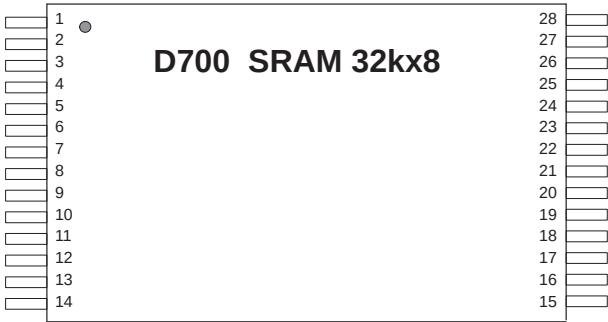
MCU (D706)

- 1 No Connection
- 2 No Connection
- 3 MCUREAD : Goes Low to indicate that the CPU is reading external address
- 4 MCU_WR : Goes Low to indicate that the CPU is writing external address
- 5 Power VL1
- 6 Ground
- 7 Ground
- 8 Connected to VL1
- 9 Connected to VL1
- 10 XSYS_RESET : A low input causes chip to reset
- 11 MCU Non Maskable Interrupt
- 12 Ground
- 13–20 MCUDA An 8-bit input/output port
- 21–28 MCUAD An 8-bit input/output port
- 29 Ground
- 30–41 MCUAD An 8-bit input/output port
- 41 MCUDA
- 42 Power VL1
- 43 XPWROFF 8-bit Timer Clock input? ? ? ?
- 44 TEMP1-EN Power Amp temperature
- 45 TEMP2-EN VCTCXO temperature
- 47 CALL LED On when phone is ringing / silent alarm
- 46 No Connection
- 48 CODEC_CLK
- 49 CODEC_DO MCU data write to Codec
- 50 CODEC_DI MCU data read from Codec
- 51 Ground
- 52 VBATDET
- 53 VCHRGMON
- 54 HOOK_RXD2 Accessory &
- 55 BTEMP Battery temperature monitoring
- 56 RFTMP 1 for PA , 2 for VCTCXO
- 57 BTYPE Battery type and size
- 58 RSSI Amps received signal strenght indicator
- 59 JCONN External audio input from accessories or external handsfree microphone
- 60 VREF

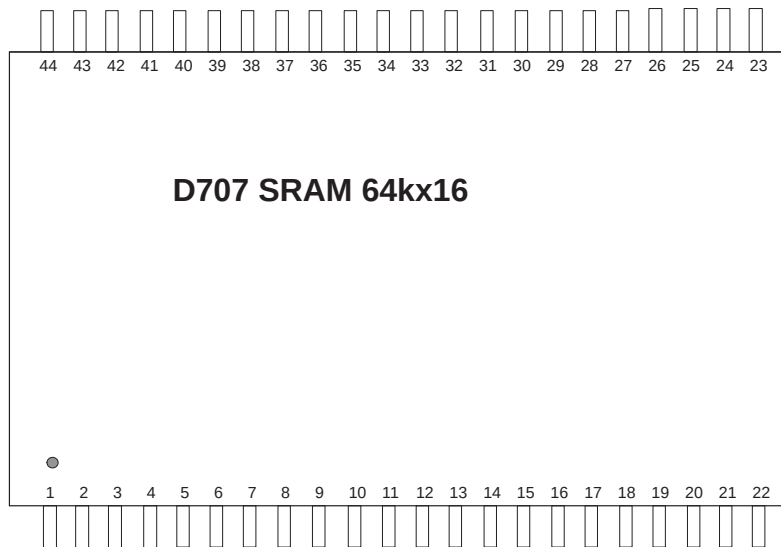


- 61 BACKLIGHT Keypad backlight on
- 62 XCODEC_CS Codec chip select
- 63 PHFS_TXD2 Power Hans Free / Flash data
- 64 HOOK_RXD2 Accessory on/off / Flash data
- 65 Vibra battery controlling
- 66 MBUS OUT Prosessor monitores outsend data
- 67 MBUSDET Mbus monitoring during sleepmode
- 68 No Connection
- 69 MCU_CLK Clock 15.36 MHz
- 70 No Connection
- 71 Ground
- 72 No Connection
- 73 No Connection
- 74 VAHS provides power to Headset
- 75 5VOFF to 4.7V Regulator (D500)
- 76 VCHRGPWR controls charging current
- 77 MCU_INT0
- 78 No Connection
- 79 VOLTLIM for future use based on charging
- 80 XMCU_AS

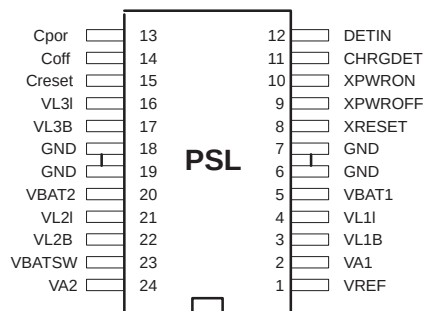
MCU memory Flash (D709), EEPROM (D703), SRAM (D700)



DSP memory (D707)



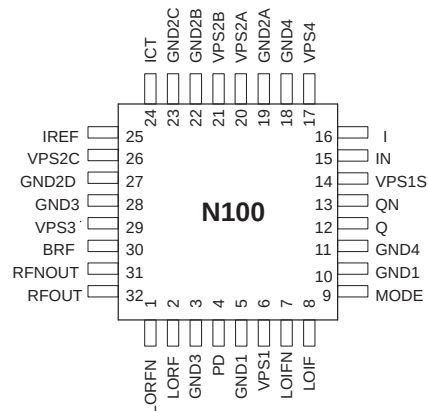
PSL + (N500)



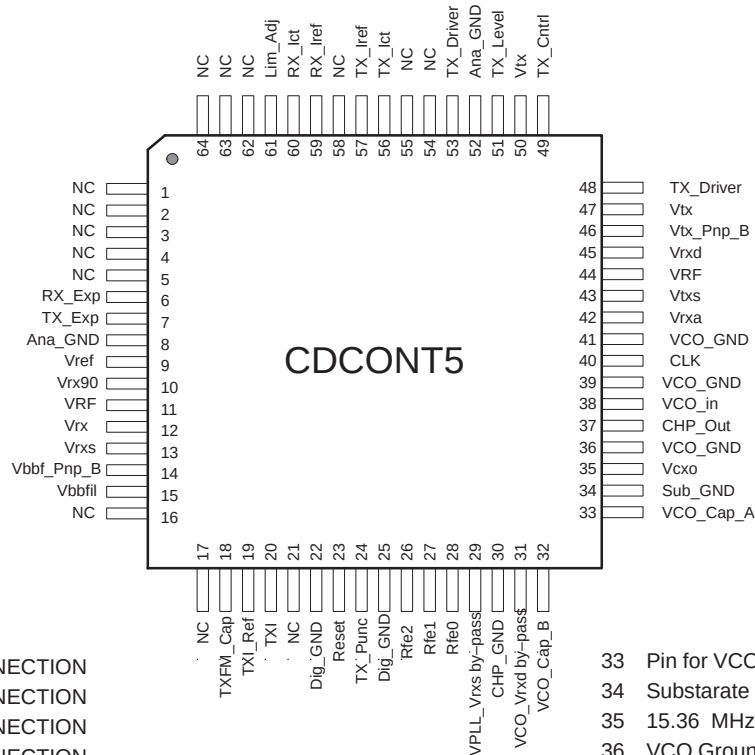
NOTE: names beginning with X indicate ACTIVE LOW operation

XPWRON input has internal pull-up resistor
XPPWROFF input has internal pull-down resistor

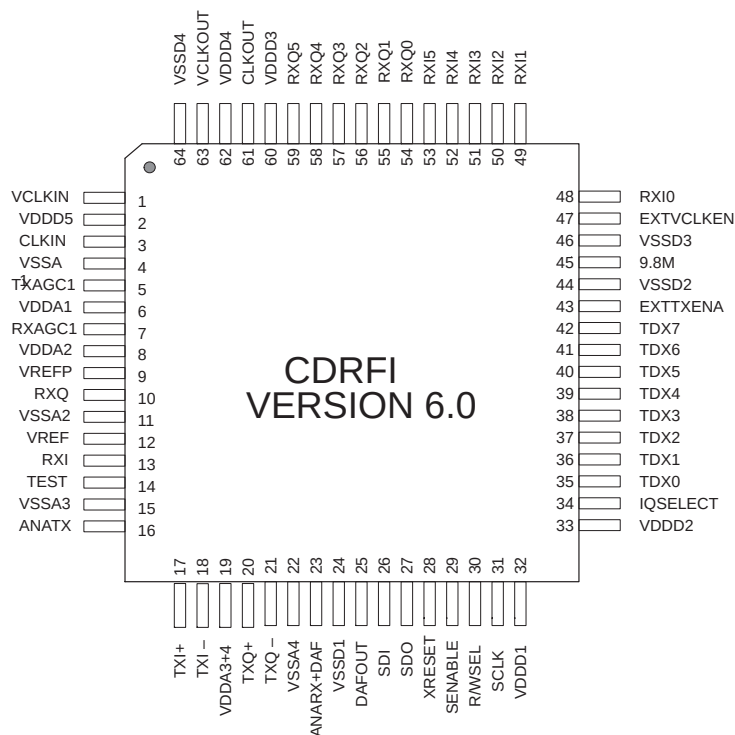
- | | | |
|----|----|--|
| 13 | 12 | 1 VREF Voltage REFERENCE output (5mA, "2% |
| 14 | 11 | 2 Analog voltage output |
| 15 | 10 | 3 Base current supply for external transistor (VL1) |
| 16 | 9 | 4 Output voltage sense from external transistor (VL1) |
| 17 | 8 | 5 VBATTERY battery voltage |
| 18 | 7 | 6 Ground (analog/logic) |
| 19 | 6 | 7 Ground (analog/logic) |
| 20 | 5 | 8 XPWR_RESET reset control signal to ASIC |
| 21 | 4 | 9 XPWROFF control input from the MCU |
| 22 | 3 | 10 XPWRON power on control from UI |
| 23 | 2 | 11 Battery CHaRGeR DETection |
| 24 | 1 | 12 DETection INput for the supply voltage monitored |
| | | 13 Connection for an external Capasitor for controlled Power-ON master Reset |
| | | 14 Connection for an external timing Capasitor defining Power-OFF delay |
| | | 15 Connection for an external timing Capasitor defining Reset signal delay |
| | | 16 Output voltage sense from external transistor (VL2) |
| | | 17 Base current supply for external transistor (VL3) |
| | | 18 Ground (analog/logic) |
| | | 19 Ground (analog/logic) |
| | | 20 Battery Voltage |
| | | 21 Output voltage sense from external transistor (VL2) |
| | | 22 Base current supply for external transistor (VL2) |
| | | 23 VBATDET SWitched VBAT voltage |
| | | 24 VA2 Analog voltage output (80mA) |

CDAGCT4 (N100)

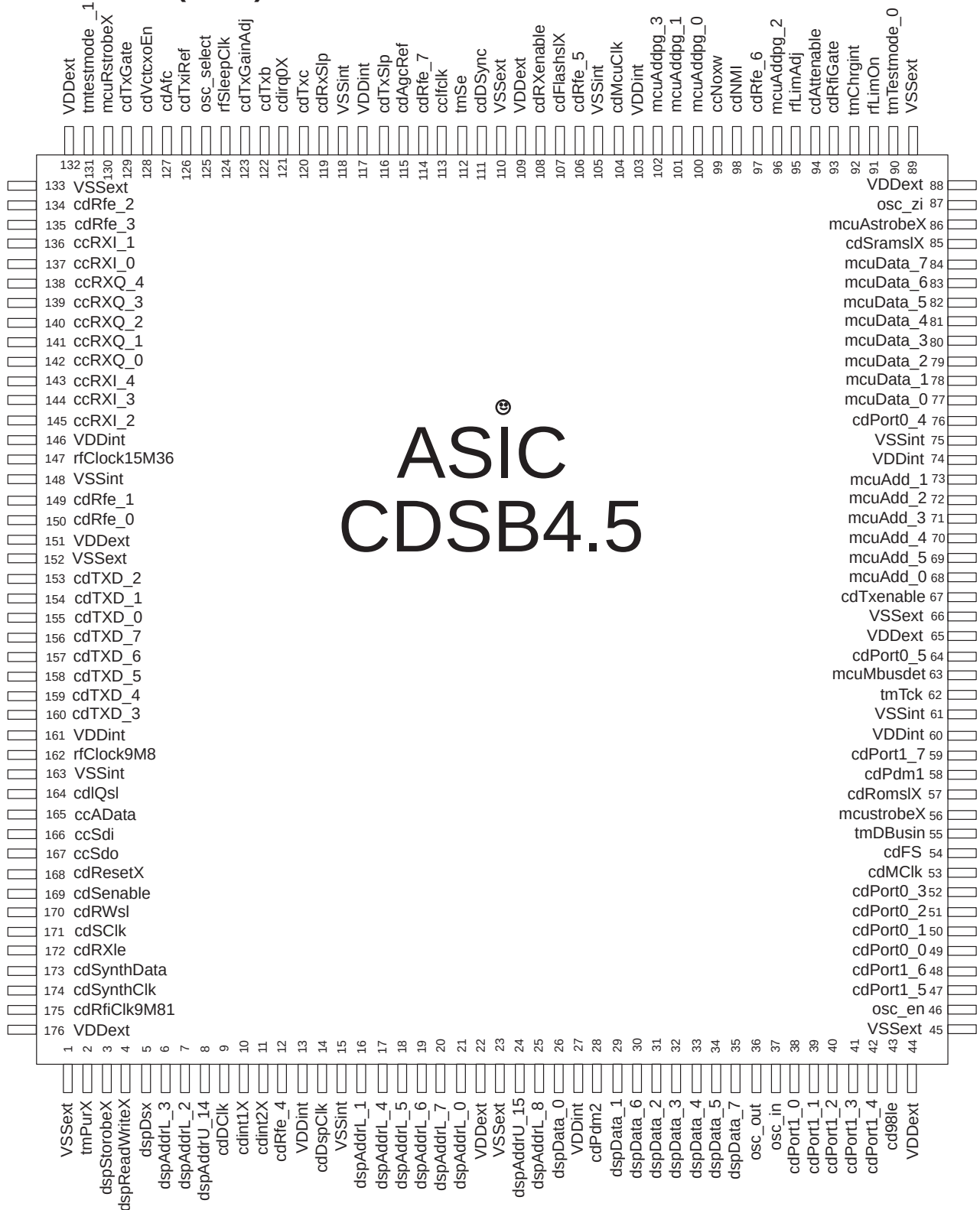
- | | |
|---|---|
| 1 180° LO for RF Mixer (Ground with cap) | 17 DC Power for I/Q Modulator |
| 2 TX_LO 0° LO for RF Mixer | 18 GROUND (Return for I/Q Modulator) |
| 3 GROUND (Return for RF Mixer and Power Amp) | 19 GROUND (Return for first CCGA) |
| 4 TX_PUNC Control for active/power-down modes | 20 DC Power for first CCGA and Gain Control Circuitry |
| 5 GROUND (Return for IF LO circuitry) | 21 DC Power for second CCGA |
| 6 DC power for IF LO circuitry | 22 GROUND (Return for second CCGA) |
| 7 180MHz 2*IF Frequency Input (Ground with cap) | 23 GROUND (Return for third CCGA) |
| 8 180MHz 0° 2*IF Frequency Input | 24 TX_ICT Input control current |
| 9 RFE2 Mode select (Between CDMA and Analog) | 25 TX_IREF Input control current reference |
| 10 GROUND (Return for IF LO circuitry) | 26 DC Power for third CCGA |
| 11 GROUND (Return for IF I/Q Modulator) | 27 GROUND Return for Gain Control circuits |
| 12 TX_Q_P 0° Baseband 'QUAD PHASE' input | 28 GROUND (Return for RF Mixer and Power Amplifier) |
| 13 TX_Q_N 180° Baseband 'QUAD PHASE' input | 29 DC power for RF mixer |
| 14 DC Power for Standby circuitry | 30 Bypass pin for Mixer Bias (Ground with cap) |
| 15 TX_I_P 180° Baseband 'IN PHASE' Input | 31 180° RF Output |
| 16 TX_I_N 0° Baseband 'IN PHASE' Input | 32 0° RF Output |

CDCONT5 (N201)

- | | |
|---|---|
| 1 NO CONNECTION | 33 Pin for VCO capacitor |
| 2 NO CONNECTION | 34 Substrate Ground |
| 3 NO CONNECTION | 35 15.36 MHz clock reference |
| 4 NO CONNECTION | 36 VCO Ground |
| 5 NO CONNECTION | 37 Charge Pump Output |
| 6 Input to RX Multiplier from RX_dB | 38 VCO input from CHP_Out |
| 7 Input to TX Multiplier from TX_dB | 39 VCO Ground |
| 8 Analog Ground | 40 9.8304 MHz clock output |
| 9 Reference voltage output | 41 VCO Ground |
| 10 Regulated voltage for the 90 MHz Frequency | 42 Regulated Voltage for the AMPS circuits |
| 11 Battery voltage supply | 43 Regulated Voltage for the TX LO buffer |
| 12 Regulated Voltage for the Receiver RF Circuits | 44 Battery voltage supply |
| 13 Regulated Voltage for Chrystal Osc and internal Decode logic | 45 Regulated Voltage for the AGC circuits CDAGCR & CDCONT |
| 14 Pin for external PNP Base connection for Vbbfil | 46 Pin for external PNP Base connection for Vtx |
| 15 Regulated voltage for the BBFIL | 47 NO CONNECTION |
| 16 NO CONNECTION | 48 NO CONNECTION |
| 17 NO CONNECTION | 49 NO CONNECTION |
| 18 Switch output | 50 Regulated voltage for the Transmitter circuits and CDAGCT (Pin 47) |
| 19 Reference input to Error Amp. | 51 Output of Driver for Power Amp. |
| 20 Transmitter power-level information | 52 Analog Ground |
| 21 NO CONNECTION | 53 Negative input of the Driver circuit for Power Amp. (Pin 48) |
| 22 Digital Ground | 54 NO CONNECTION |
| 23 Digital control bit for Regulator switching | 55 NO CONNECTION |
| 24 Digital control bit for Regulator switching | 56 Control current for CDAGCT |
| 25 Digital Ground | 57 Reference current for CDAGCT |
| 26 Digital control bit for Regulator switching | 58 NO CONNECTION |
| 27 Digital control bit for Regulator switching | 59 Reference current for CDAGCR |
| 28 Digital control bit for Regulator switching | 60 Control current for CDAGCR |
| 29 Vrx by-passed supply for PLL digital logic | 61 Indicator for Limiter |
| 30 Ground for Charge Pump circuit | 62 NO CONNECTION |
| 31 Vrx by-passed supply for VCO and Clock Buffer | 63 NO CONNECTION |
| 32 Pin for VCO capacitor | 64 NO CONNECTION |

CDRFI (N700)

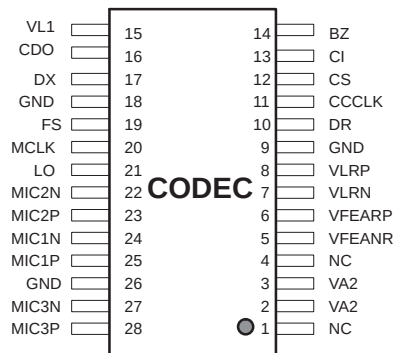
1 15.36MHz VCLock recovery INput	17 TX_I_P TX signal In-phase +	33 Digital Power VL3
2 Digital Power VL3	18 TX_I_N TX signal In-phase -	34 CDRFI_IQSEL TX IQ SELECT
3 9.83MHz CLock recovery INput	19 Analog Power VL3	35-42 TXD TX Data bit 0-7
4 Analog Ground	20 TX_Q_P TX signal Quadrature-phase +	43 CDRFI_GATE EXTernal TX ENABLE
5 TX_GAIN TX AGC control	21 TX_Q_N TX signal Quadrature-phase -	44 Digital Ground
6 Analog Power VL3	22 Analog Ground	45 CDRFI_9.8MHz clock
7 RX_GAIN RX AGC control	23 DAF ANALog mode RX+DAF signal	46 Digital Ground
8 Analog Power VL3	24 Analog Ground	47 VCO_EN EXTernal VCLK ENABLE
9 Positive Voltage REFerence bypass	25 DAF OUTput	48 No Connection
10 RX_Q RX signal Quadrature-phase	26 CDRFI_SI Serial data In	49-53 RXI RX In-phase data bit 1-5
11 Analog Ground	27 CDRFI_SO Serial data Out	54 No Connection
12 Voltage REFerence bypass	28 XSYS_RESET Whwen set = 0	55-59 RXQ RX Quadrature-phase data bit 1-5
13 RX_I RX signal In-phase	29 CDRFI_SEN Serial data ENABLE	60 Digital Power VL3
14 TEST input (Not used)	30 CDRFI_RWSEL Read/Write SElect	61 9.38M_IN CLock recovery OUTput
15 Analog Ground	31 CDRFI_SCLK Serial data CLock	62 Digital Power VL3
16 MOD ANALog mode TX signal	32 Digital Power VL3	63 V15.36M_IN CLock recovery OUTput
		64 Digital ground

CDSB 4.5 (D704)

ASIC CDSB 4.5

1 GND	65 VL1	122 TXB PDM output signal
2 XPWR_RESET Power on Reset	66 GND	123 RX_OFFSET PDM
3 XDSP_STRB DSP External memory strobe	67 No Connection	124 Sleep Clock
4 DSP_RXW DSP Write enable	68-73 MCUAD MCU Lower address bus	125 Connected to VL1
5 XDSP_DS DSP data select	74 VL1	126 TXI_REF PDM output signal
6-8 DSPAD DSP Lower address	75 GND	127 AFC PDM output signal
9 DSP_MCLK DBUS 512KHz Clock	76 No Connection	128 VCO_EN VCTCXO enable
10 DSP_CLK DSP Interrupt request 0	77-84 MCUDA MCU Data bus	129 TX_PUNC Signal to turn off TX
11 DSP_CLK DSP Interrupt request 1	85 XSRAM SRAM select bit	130 XMCU_RD Read enable
12 RX_FIL_CAL Output sourcing rRX_FIL signal	86 XMCU_AS MCU Address valid strobe	131 Connected to GND
13 VL1	87 No Connection	132 VL1
14 DSP_CLK DSP clock output 15.36MHz	88 VL1	133 GND
15 GND	89 GND	134 RF_RFEN2 Power control to CDCONT
16-21 DSPAD DSP Lower address	90 Connected to GND	135 FAST Output sourcing rfFast signal
22 VL1	91 No Connection	136,137 RXI_ Receive I data
23 GND	92 CHRGI_INT Charge interrupt	138-142 RXQ Receive Q data
24-25 DSPAD DSP Upper address	93 CDRFI_GATE Signal to control Transmitt mode with in CDRFI	143-145 RXI_ Receive I data
26 DSPDA DSP data bus	94 SWAGC Signal to control gain switching	146 VL1
27 VL1	95 Tx power greater than that set by TXI_REF	147 15.36M_IN Clock
28 No Connection	96 MCUAD MCU Upper address bus	148 GND
29-35 DSPDA DSP data bus	97 No Connection	149 RFEN1 Power control to CDCONT
36 32.768KHz Clock osc. circuit	98 MCU_NMI Non Maskable interrupt	150 RFEN0 Power control to CDCONT
37 32.768KHz Clock osc. circuit	99 No Connection	151 VL1
38-42 LCD_COL GPIO port 1	100-102 MCUAD MCU Upper address bus	152 GND
43 No Connection	103 VL1	153-160 TXD_ Multiplexed Tx I/Q data in dig mode Bidirectional transfer of data in dig mode
44 VL1	104 MCU_CLK Clock output 15.36MHz	161 VL1
45 GND	105 GND	162 9.83M_IN Clock
46 Connected to VL	106 No Connection	163 GND
47-52 LCD_COL GPIO port 1	107 XFLASH_CS Flash select bit	164 CDRFI_IQSEL IQ select signal in dig mode Address select bit in anal mode
48 GPIO Port 1	108 No Connection	165 DAFOUT Analog mode input data
49-52 GPO port 0	109 VL1	166 CDRFI__SI Serial data output pin
53 CODEC_MCLK Codec clock 512KHz	110 GND	167 CDRFI__S0 Serial data input pin
54 CODEC_FS Codec Sync 8KHz	111 DSP_SYNC DBUS 8KHz Sync Clock	168 XSYS_RESET System reset signal
55 DBUS Line in	112 Connected to GND	169 CDRFI__SEN Serial data enable
56 XMCU_WR MCU Write enable	113 No Connection	170 CDRFI_RWSEL Read/Write select in anal mode
57 XROM_CS ROM select bit	114 RX_CAL Output sourcing rRX_CAL signal	171 CDRFI_SCLK Serial data clock
58 No Connection	115 AGC_REF Auxilliary AGC PDM	172 RX_LE RX Synthesizer enable
59 No Connection	116 TX_SLOPE PDM	173 DATA RX Synthesizer serial data
60 VL1	117 VL1	174 CLK Synthesizer serial clock
61 GND	118 GND	175 CDRFI_9.8M Clock
62 Connected to VL1	119 RX_SLOPE PDM	176 VL1
63 MBUSDET Mbus activity detect	120 TX_OFFSET PDM	

AUDIO CODEC (N600)



- 1 Not connected
- 2 VA2 Power supply for the analog section
- 3 VA2 Power input for power section
- 4 Not connected
- 5 Not connected
- 6 XEAR_HFJPWR External earpiece output VF+
- 7 EarN Differential / earpiece amp outputs
- 8 EarP Differential / earpiece amp outputs
- 9 Power Ground
- 10 PCMIN Receive data input
- 11 CODEC_CLK Control Clock Input
- 12 XCODEC_CS Chip Select Input
- 13 CODEC_DI Control data Input
- 14 BUZZER Pulse width modulated buzzer driver output

- 15 VL1 Power supply input for the digital section
- 16 CODEC_DO Control Data output
- 17 PCM Transmit data output
- 18 Digital Ground
- 19 CODEC_FS Frame Synch Input
- 20 CODEC_MCLK Master Clock Input
- 21 MICENX A logic written into DO (CR1) appears at LO pin as logic 0 (and vice versa)
- 22 2nd neg high impedance input to transmit pre-amplifier microphone connection (Connected via cap to Ground)
- 23 XMIC_JCONN 2nd pos high impedance input to transmit pre-amplifier microphone connection
- 24 MicN Neg high impedance input to transmit pre-amplifier microphone connection
- 25 MicP Pos high impedance input to transmit pre-amplifier microphone connection
- 26 Analog Ground
- 27 3th neg high impedance input to transmit pre-amplifier microphone connection (Connected via cap to Ground)
- 28 3th pos high impedance input to transmit pre-amplifier microphone connection (Connected via cap to Ground)

DSP (D705)

